APPLICATION

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TITLE: TRANSITION ENCODED DYNAMIC BUS CIRCUIT

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TRANSITION ENCODED DYNAMIC BUS CIRCUIT

BACKGROUND

[0001] Dynamic CMOS interconnect drivers may be substituted for static CMOS drivers in high performance on-chip buses. In buses with static drivers, when neighboring wires switch in opposite directions, e.g., from Vss to Vcc on one wire and from Vcc to Vss on its neighbor, the voltage swing on the parasitic capacitor which exists inherently between the two wires is not Vcc-Vss. Rather, the voltage swing seen by the parasitic capacitor is doubled to (Vcc-Vss)*2. Due to the Miller effect, the effective capacitance seen by the wire is doubled, yielding a Miller Coupling Factor (MCF) of 2.0.

[0002] In buses with dynamic drivers, all wires are reset to a pre-charge state (for example, Vss) in a pre-charge portion of the clock cycle, and then may either remain at that state or switch to an opposite state (Vcc in this example) in an evaluate portion of the cycle. Since all wires in the bus are pre-charged to the same state, two neighboring wires cannot switch in opposite directions during evaluation, and the maximum voltage swing on the terminals of the parasitic capacitor between the two wires will be (Vcc-Vss). Thus, the MCF is reduced from 2.0 in

static CMOS drivers to 1.0 in dynamic CMOS drivers, thereby reducing a large component of the wire's worst-case effective coupling capacitance.

[0003] A trade-off is that dynamic buses may consume more power than static buses. Because dynamic buses are reset to the pre-charge state each cycle, the power used by the bus depends on the actual value of the input, unlike static buses, which draw power only when the input value transitions. Thus, a dynamic bus will continue to use power for as long as the input value is HIGH, whereas a static bus would not.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] Figure 1 is a block diagram of a transition encoded dynamic bus circuit according to an embodiment.

[0005] Figure 2 is a schematic diagram of an encoder circuit according to an embodiment.

[0006] Figure 3 is a schematic diagram of a decoder circuit according to an embodiment.

DETAILED DESCRIPTION

[0007] Figure 1 illustrates an encoded dynamic bus 100 according to an embodiment. The bus includes multiple bus lines 102. The bus lines may be arranged as domino data paths, each bus line including a dynamic driver 104 at the

input node 106, a series of inverting stages 108, each stage including a CMOS inverter 110 and a wire resistance 112, and a clocked flip flop (FF) 114 at the output node 116. A dynamic bus repeater 120 in the middle of the bus line divides the bus line into a front segment 122 and a rear segment 124.

[0008] An encoder circuit 130 may be provided at the front end of the bus line 102, coupled to the output node of the dynamic driver 104. A decoder circuit 132 may be provided at rear end of the bus line 102, coupled to the input node of the clocked FF 114. The encoder circuit translates transition activity at the input into an output logic state. Instead of a LOW input causing a LOW output, a LOW output in an exemplary transition encoding scheme indicates that no transition has occurred on the input. A HIGH output indicates that the input has transitioned from LOW to HIGH, or from HIGH to LOW in the exemplary encoding scheme. The decoder 132 then uses this encoded signal to reconstruct the original input to the encoder. By hiding the actual input value from the rest of the bus line and only indicating a transition on the input, the encoder scheme may reduce power consumed by the dynamic bus.

[0009] Figure 2 illustrates an encoder circuit 200 according to an embodiment. A domino gate 202 includes an

input transistor 204 controlled by the data input to the bus line 102. A domino gate 206 includes an input transistor 208 controlled by the value of the data input to the bus on the previous cycle, and supplied by a clocked FF 210, which stores the complement of the previous data input value. The domino gates 202 and 206 are clocked by a $\Phi 1$ clock signal, and the clocked FF 210 is clocked by the complement of the $\Phi 1$ clock signal, $\overline{\Phi 1}$.

[0010] During pre-charge, when $\Phi 1$ is LOW and $\overline{\Phi 1}$ is HIGH, node A, node B, and node C are all HIGH. The value on node A depends on the value of the current data input, and the value on node B depends on the value of the previous data input.

[0011] During evaluate, $\Phi 1$ rises and node A and node B conditionally transition to a LOW value, depending upon the current and previous inputs, respectively. As they fall, node C will also fall if nodes A and B exhibit different behavior, that is, one node falls while the other remains high. The value on node C is then inverted and driven onto the interconnect bus line. When $\Phi 1$ falls, the clocked FF 210 is triggered to latch the current data for the next cycle.

[0012] Consider the case when the data signal does not transition, and remains LOW in the previous and current cycles. When $\Phi 1$ rises, the PMOS transistors 220 in the domino gates 202 and 206 turn off, and the NMOS transistors 222 turn on. Since the signals on both input NMOS transistors 204 and 208 are low, both transistors remain OFF. Thus, the path to Vss through NMOS transistors 220 are closed, and the values on nodes A and B remain HIGH. With no discharge path for node C, the value on node C remains HIGH, which is inverted by an inverter 230. The encoder 200 outputs a LOW signal to the bus line 102, indicating that no transition has occurred at the input to the bus line.

[0013] Another case in which the input does not transition is when the input to the bus remains HIGH in the previous and current cycles. In this case, both input transistors 204 and 208 turn on, opening a discharge path for the signals on nodes A and B. As the signals on nodes A and B transition from HIGH to LOW, the NMOS transistors 240 and 242 below node C turn off, thereby closing the discharge path from node C to Vss through the domino gates 202 and 206. Also, the PMOS transistors 244 and 246 turn on in response to the signals on nodes A and B transitioning LOW. This opens the path to Vcc and pulls

node C HIGH. This signal is inverted and a LOW signal is output to the bus line, again indicating no transition at the input.

[0014] The encoder 200 will output a HIGH signal to the bus if the data input transitions from LOW to HIGH or HIGH to LOW between the previous and current cycles. For example, if the data signal transitions from LOW to HIGH, the input transistor 204 on the domino gate 202 will turn on, and the input transistor 206 on the domino gate 204 coupled to the clocked FF 210 will remain off. When $\Phi 1$ rises, node A will fall from HIGH to LOW, causing the PMOS transistor 244 to turn on and the NMOS transistor 242 to turn off. Node B will remain HIGH, causing the PMOS transistor 246 to remain OFF and the NMOS transistor 240 to remain ON. The states of these transistors 246 (OFF) and 240 (ON) close the path to Vcc and open a discharge path to Vss, respectively, for the node C. Consequently, the node C will be pulled LOW, and the encoder will output a HIGH signal to the bus, indicating a transition at the input.

[0015] Alternatively, if the data signal transitions from HIGH to LOW, the input transistor 204 on the domino gate 202 will remain off, and the input transistor 206 on the domino gate 204 coupled to the clocked FF 210 will turn on. When $\Phi 1$ rises, node A will remain HIGH, causing the

PMOS transistor 244 to remain OFF and the NMOS transistor 242 to remain ON. Node B will fall from HIGH to LOW, causing the PMOS transistor 246 to turn on and the NMOS transistor 240 to turn off. The states of transistors 244 (OFF) and 242 (ON) close the path to Vcc and open a discharge path to Vss, respectively, for the node C. Consequently, the node C will be pulled LOW, and the encoder will output a HIGH signal to the bus, indicating a transition at the input.

[0016] Figure 3 illustrates a decoder circuit 300 according to an embodiment. The decoder 300 includes a clocked FF 302, which stores the encoded signal input from the bus on the previous cycle. The FF 302 is clocked by the $\Phi 1$ signal, which hides the pre-charge signal placed on the bus each cycle from the FF 302, and hence the decoder 300. The encoded signal input from the bus, at a node D, is coupled to the gates of a PMOS transistor 304 and an NMOS transistor 306. The PMOS transistor 304 is connected between the input of the clocked FF 302, at a node E, and the output of the clocked FF 302, at a node F. The signal on node F controls an NMOS transistor 308 and a PMOS transistor 310, which is connected between nodes D and E. The signal on node F is inverted by an inverter 312, the

output of which controls an NMOS transistor 314 connected between nodes D and E.

[0017] When node D (from the bus) is LOW, the PMOS transistor 304 turns on, providing a path between nodes E and F. When node F (from FF 302) is LOW, the transistors 310 and 314 turns on, providing a path between nodes D and E. When both nodes D and F are LOW, both pull-down NMOS transistors 306 and 308 will be ON, providing a discharge path from node E to Vss.

[0018] The output of the decoder 300 will transition each cycle in which the signal on the input to the bus transitions. Table 1 illustrates an exemplary encoding/decoding operation.

Encoder			Decoder	
IN	PREV	BUS	FF	OUT
0	0	0	0	0
1	0	1	0	1
0	1	1	1	0
0	0	0	0	0
1	0	1	0	1
1	1	0	1	1

Table 1

[0019] As shown in Table 1, each transition at the input to the bus results in a transition at the output of the bus. The transition provides information as to whether there was a transition at the input, regardless of the actual value on the input to the bus, or the value stored in the FF 302 in the decoder 300.

[0020] The decoder must distinguish between a LOW to HIGH transition and a HIGH to LOW transition. This may be accomplished by maintaining synchronized state information in both the encoder 130 and the decoder 132.

[0021] The encoding scheme described above may reduce the power consumed by the dynamic bus to levels comparable to that of static buses. While the addition of the encoding and decoding circuits may produce an additional delay, the overhead is relatively small, and the bus may maintain most of the performance advantages associated with dynamic buses.

[0022] A number of embodiments have been described. Nevertheless, it will be understood that various modifications may be made without departing from the spirit and scope of the invention. For example, circuits other than those shown in Figures 2 and 3 may be used to implement the XOR operations utilized in the encoding and

decoding operations. Accordingly, other embodiments are within the scope of the following claims.